



PH2925U

N-channel TrenchMOS ultra low level FET

Rev. 03 — 29 November 2005

Product data sheet

1. Product profile

1.1 General description

Ultra low level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Low level threshold
- Low thermal resistance
- SO8 equivalent area footprint
- Low on-state resistance

1.3 Applications

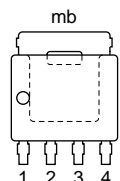
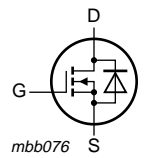
- DC-to-DC converters
- Portable applications
- Switched-mode power supplies
- Notebook computers

1.4 Quick reference data

- $V_{DS} \leq 25 \text{ V}$
- $R_{DSon} \leq 3 \text{ m}\Omega$
- $I_D \leq 100 \text{ A}$
- $P_{tot} \leq 62.5 \text{ W}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)		
4	gate (G)		
mb	mounting base; connected to drain (D)		

SOT669 (LFPAK)

PHILIPS

3. Ordering information

Table 2: Ordering information

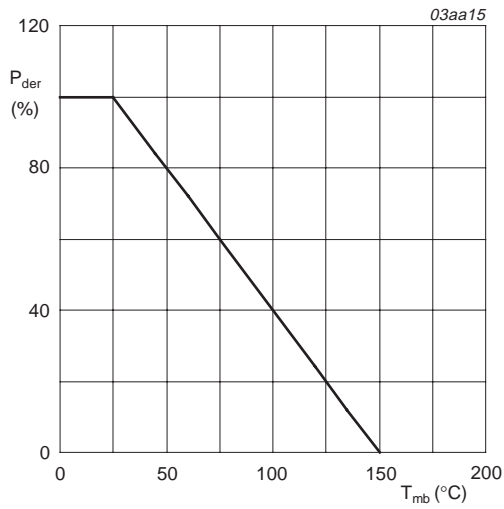
Type number	Package		Version
	Name	Description	
PH2925U	LFPAK	plastic single-ended surface mounted package; 4 leads	SOT669

4. Limiting values

Table 3: Limiting values

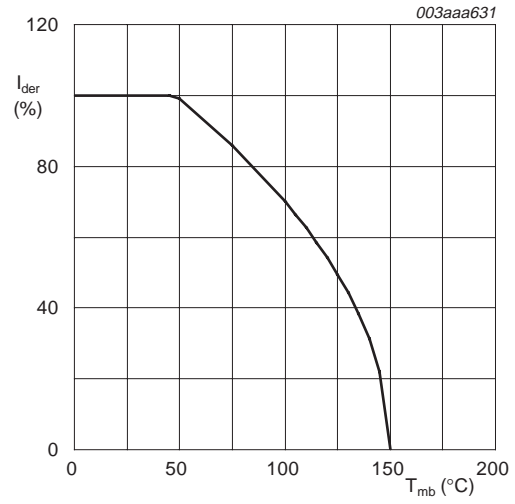
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-	± 10	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 4.5\text{ V}$; see Figure 2 and 3	-	100	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 4.5\text{ V}$; see Figure 2	-	70	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	300	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	$^{\circ}\text{C}$
T_j	junction temperature		-55	+150	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	150	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 70.7\text{ A}$; $t_p = 0.22\text{ ms}$; $V_{DS} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_j = 25\text{ °C}$	-	250	mJ



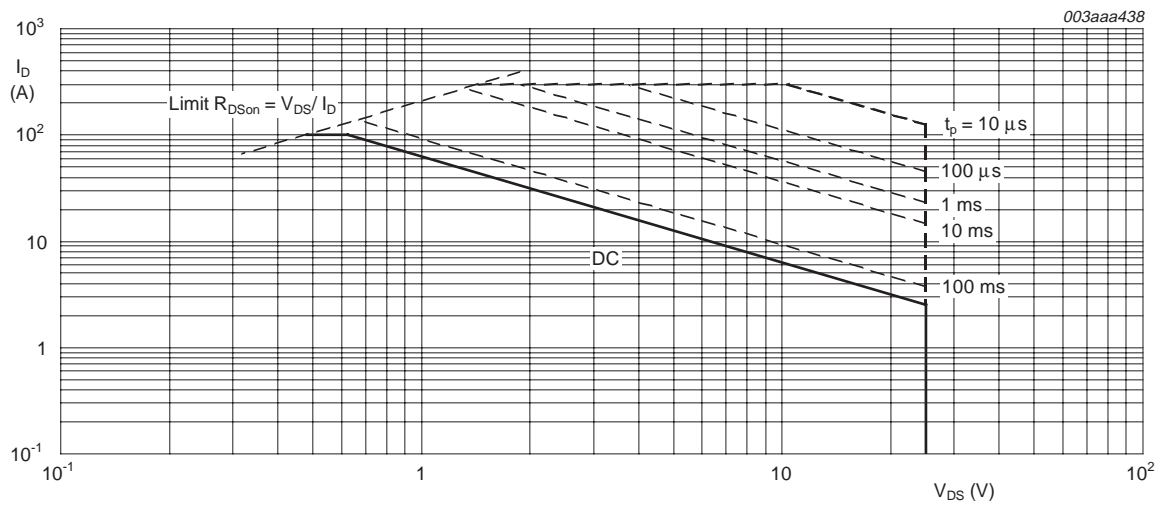
$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25\text{ }^{\circ}\text{C}$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W

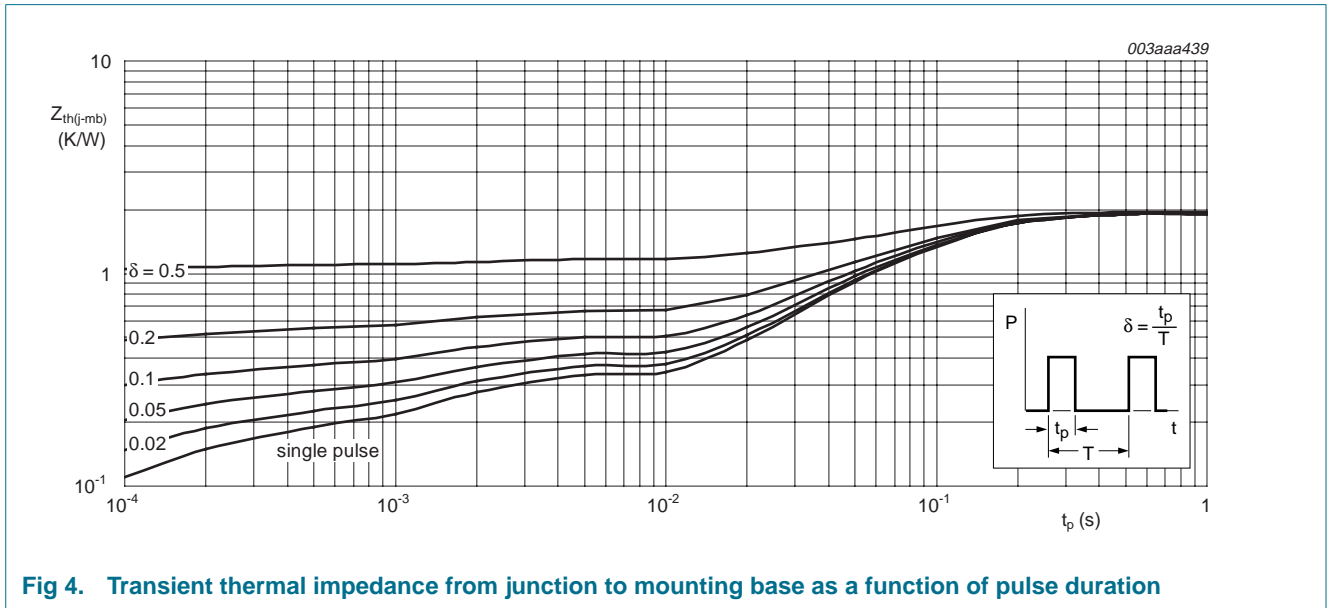
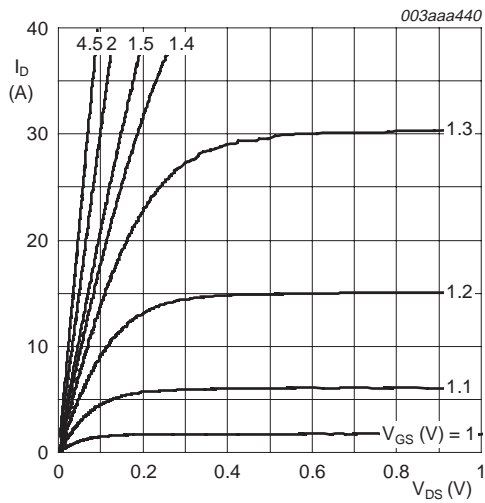


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

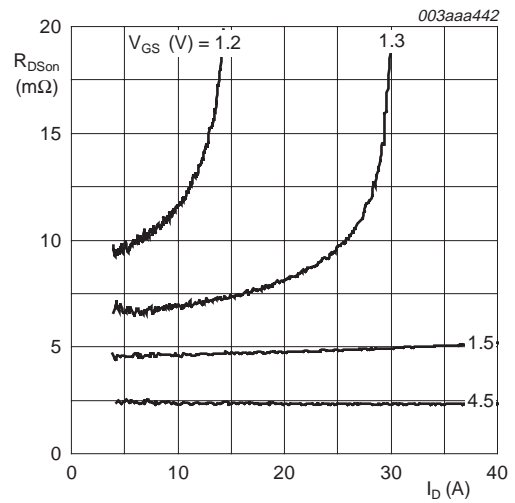
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V T _j = 25 °C	25	-	-	V
		T _j = -55 °C	22.5	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; see Figure 9 and 10 T _j = 25 °C	0.45	0.7	0.95	V
		T _j = 150 °C	0.25	-	-	V
		T _j = -55 °C	-	-	1.2	V
I _{DSS}	drain leakage current	V _{DS} = 25 V; V _{GS} = 0 V T _j = 25 °C	-	0.06	1	μA
		T _j = 150 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	-	20	100	nA
R _G	gate resistance	f = 1 MHz	-	1.55	-	Ω
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; see Figure 6 and 8 T _j = 25 °C	-	2.3	3	mΩ
		T _j = 150 °C	-	3.6	4.8	mΩ
		V _{GS} = 2.5 V; I _D = 25 A	-	3.2	4.2	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 50 A; V _{DS} = 10 V; V _{GS} = 4.5 V; see Figure 11 and 12	-	92	-	nC
Q _{GS}	gate-source charge		-	12	-	nC
Q _{GD}	gate-drain charge		-	20.2	-	nC
V _{GS(pl)}	gate-source plateau voltage		-	1.6	-	V
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 10 V; f = 1 MHz; see Figure 14	-	6150	-	pF
C _{oss}	output capacitance		-	1170	-	pF
C _{rss}	reverse transfer capacitance		-	814	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 10 V; R _L = 1 Ω; V _{GS} = 4.5 V; R _G = 4.7 Ω	-	30	-	ns
t _r	rise time		-	80	-	ns
t _{d(off)}	turn-off delay time		-	258	-	ns
t _f	fall time		-	114	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; see Figure 13	-	0.72	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; di _S /dt = -100 A/μs; V _{GS} = 0 V	-	60	-	ns



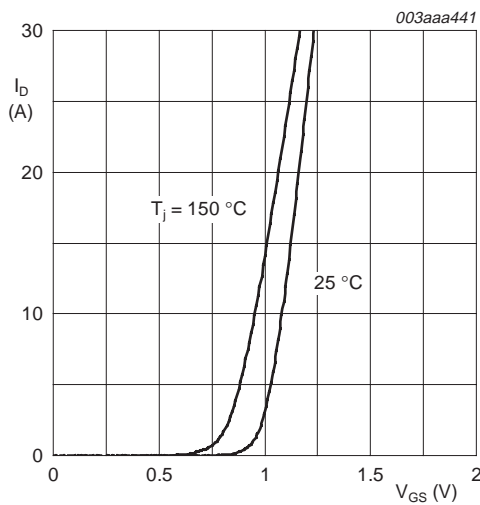
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



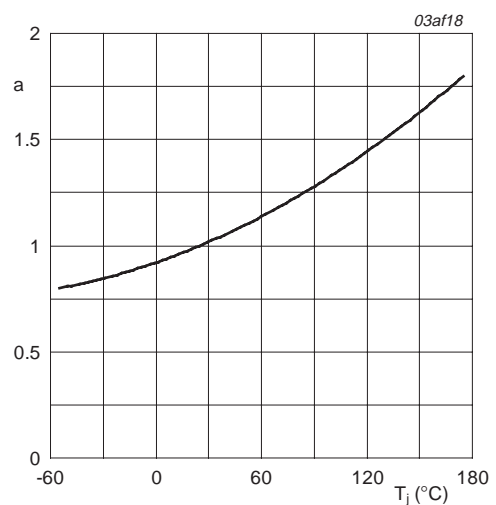
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



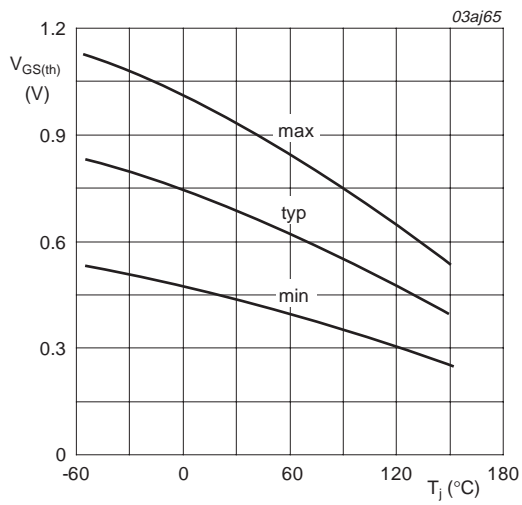
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



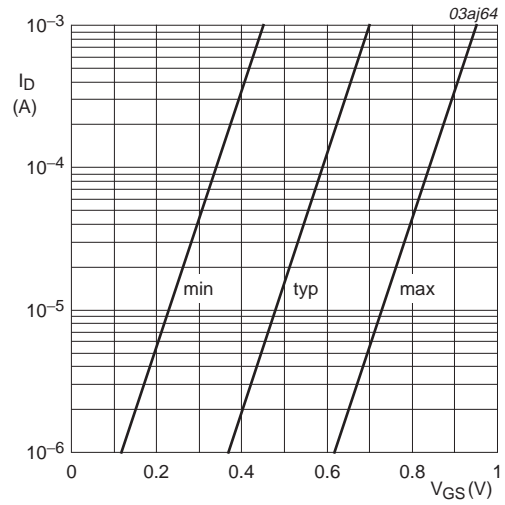
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



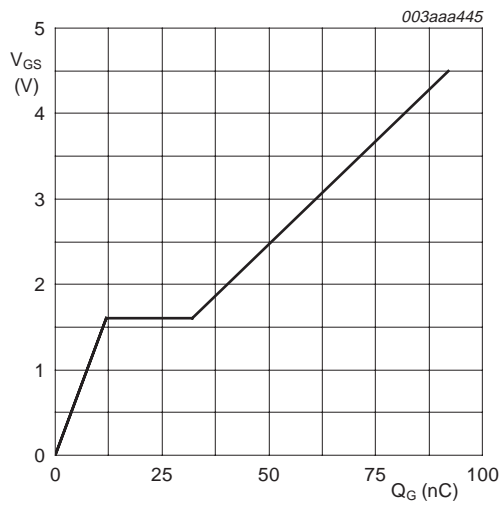
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 50 \text{ A}; V_{DS} = 10 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

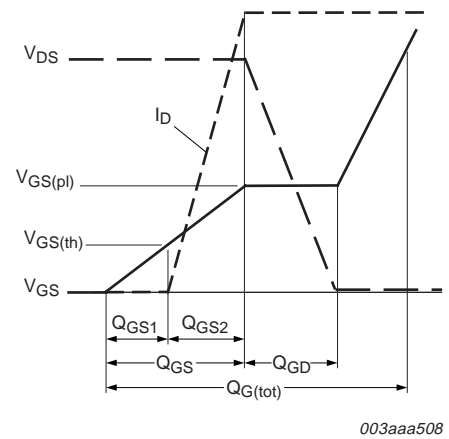
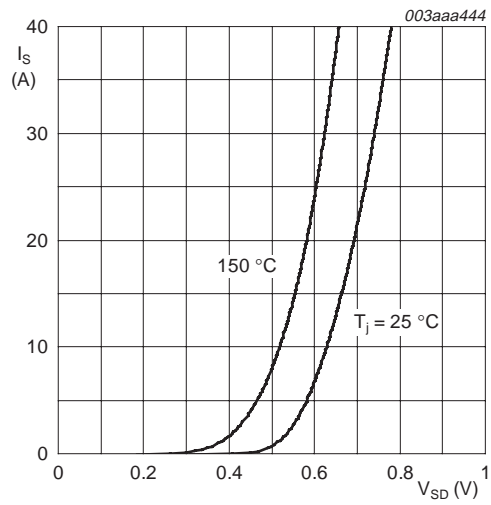
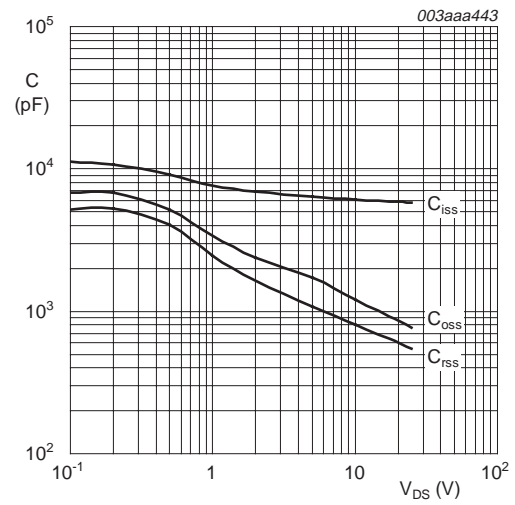


Fig 12. Gate charge waveform definitions



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



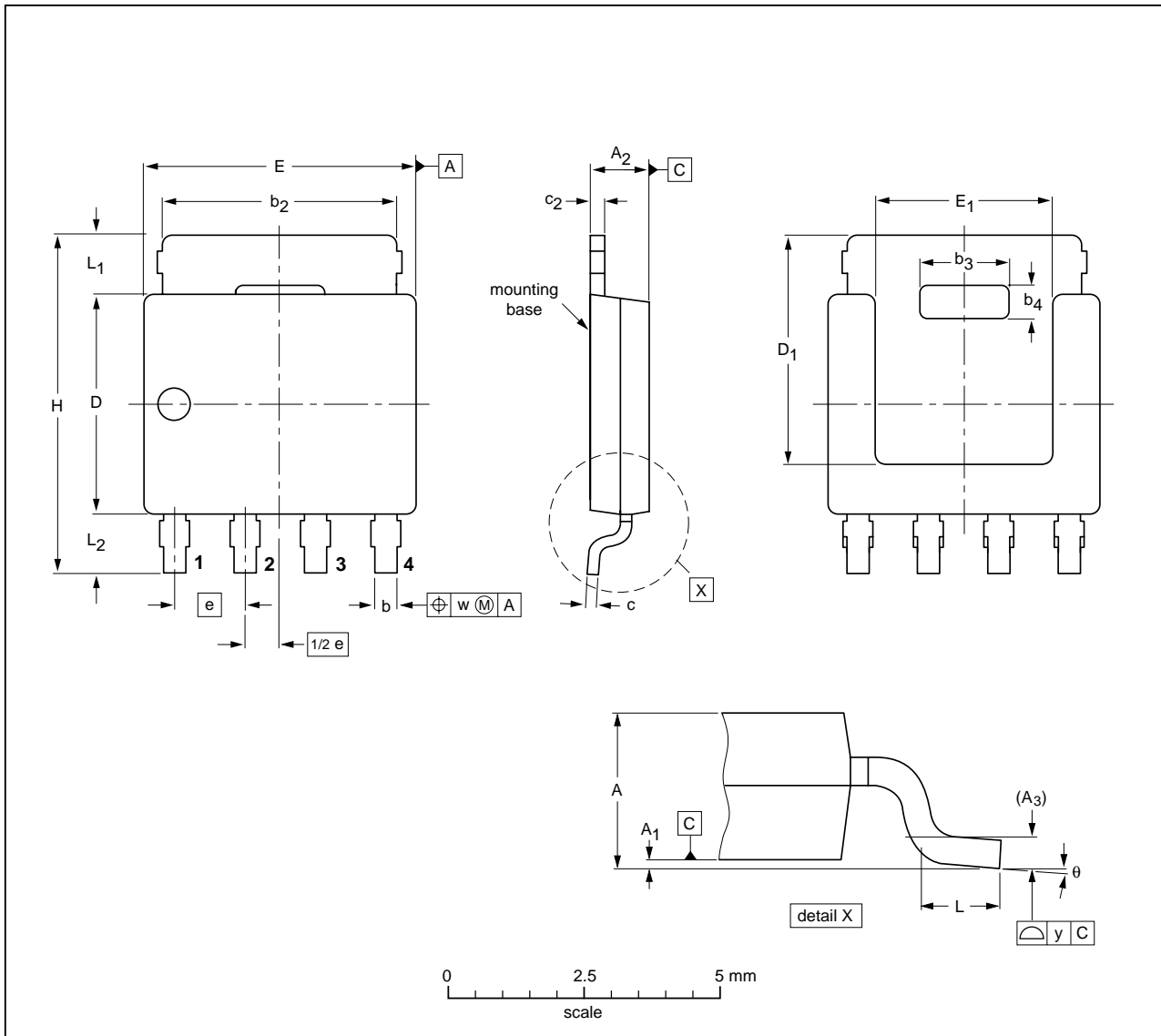
$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface mounted package (LPAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾ max	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				03-09-15 04-10-13

Fig 15. Package outline SOT669 (LPAK)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH2925U_3	20051129	Product data sheet	-	-	PH2925U-02
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 1.4 "Quick reference data": R_{DSon} value modified Section 6 "Characteristics": $V_{GS(th)}$ maximum limits, R_G and $V_{GS(pl)}$ values added. Section 6 "Characteristics": R_{DSon} maximum limits modified. Figure 5 and 6: modified 				
PH2925U-02	20040408	Product data	-	9397 750 13064	PH2925U-01
PH2925U-01	20030502	Product data	-	9397 750 11407	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
6	Characteristics	5
7	Package outline	9
8	Revision history	10
9	Data sheet status	11
10	Definitions	11
11	Disclaimers	11
12	Trademarks	11
13	Contact information	11



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